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Design with EPROMs For Future Flexibility

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by John F. Rizzo

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INTRODUCTION

Flexibility and design ease—those are the key words in today's fast paced world of microprocessor system design. We must be practical in our designs and have flexibility to accommodate larger memory densities and more useful peripherals. Such a flexible, practical approach will allow us to design-in the future today. Designing EPROM systems based on speculation of future events is indeed a risky business. Vendors introduce devices with different pinouts, varying power requirements and unique densities. A more prevalent problem is one of industry wide availability; how can one possibly implement a firm design based on precarious and unpredictable supplies? How are designers to foresee rapid advances in EPROM densities? And, what about microprocessor evolution? Why should we implement a long range design when answers to such questions are so unsure? The reasons are clear. A small additional effort now will save a complete redesign and reimplementation in the years ahead. In one particular area—EPROM memory systems—the tools are available now, today.

The following paragraphs seek to refocus present EPROM design concepts. Flexible and creative approaches that encourage straightforward system evolution will be discussed. Simple and complex decoding schemes for device selection will be detailed and various control approaches explained. Logical design configurations that permit natural density upgrades will be noted. Finally, basic calculations aimed at determining memory speed requirements are discussed. These general system concepts are intended to inform the reader of recent developments that provide greater flexibility and system understanding.

In an ideal sense a flexible design would allow the use of all possible pinouts, package sizes, control schemes, and power requirements. To accomplish such universality one would have to make available all voltage and system signals and jumper them in at each device location. Figure 1 details this jumpered implementation. Admittedly, such a design would be inefficient—nevertheless, it fulfills all of our desired goals. Several power supply voltages are available, the pinout extends addressing up to 512K bits, the package is a relatively modest 28 pins, both single and dual control schemes are available. In the remaining paragraphs an attempt will be made to preserve that flexibility while making the implementation a more practical one.

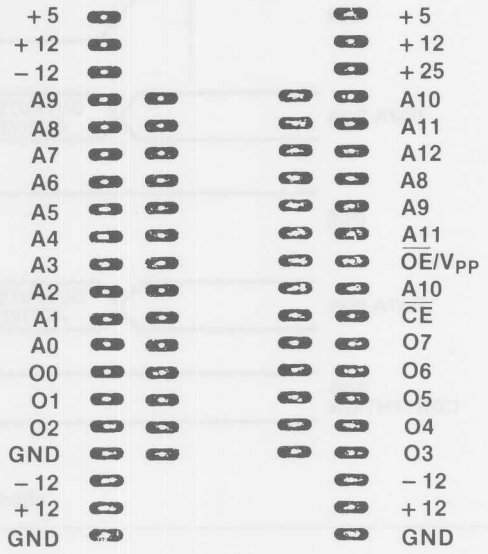


Figure 1.

BUS CONTENTION

The most fundamental decision a designer has to face involves solving the bus contention problem. Bus contention can arise when multiple devices are connected to a common data bus. If chip selection is accomplished only through address decoding then timing incompatibilities can result. The crucial timing parameters are address decode time (t_{ACC}), time from active chip enable to data valid (t_{CE}), and device deselect time (t_{DF}). Basically, contention occurs when one device is being selected while another is undergoing deselection. The worst case is when devices driving opposite logic levels are involved. A timing incompatibility results from fast decode times and relatively slow device turnoff times. Figure 2 illustrates the timing relationships while Figure 3 shows the physical circuit arrangement. The major problems that bus contention can cause are somewhat subtle in nature. Current and voltage spiking on the power supply rails is the most measurable one. Such noise can lead to a whole host of problems including invalid data, false triggering, race conditions, and reflections. In low performance systems these phenomena may have little effect—however—higher speed CPUs and mainframes can certainly be affected. Figure 4 shows a photograph of bus contention and its effects on circuit voltages and currents. Typically, the system designer solves the contention problem by making worst case timing calculations of decoder delays and EPROM turnoff times. Unfortunately, these parameters are subject to wide variation over time and temperature and correct designs on paper may not function in a realistic environment. When multiple cards with fast RAMs and PROMs are connected to a common bus the calculation and interaction becomes extremely complex. Schemes for device selection that rely only on decoded addresses (single line control) require intensive design efforts, with less than sure results. These schemes are thus prime candidates for bus contention problems.

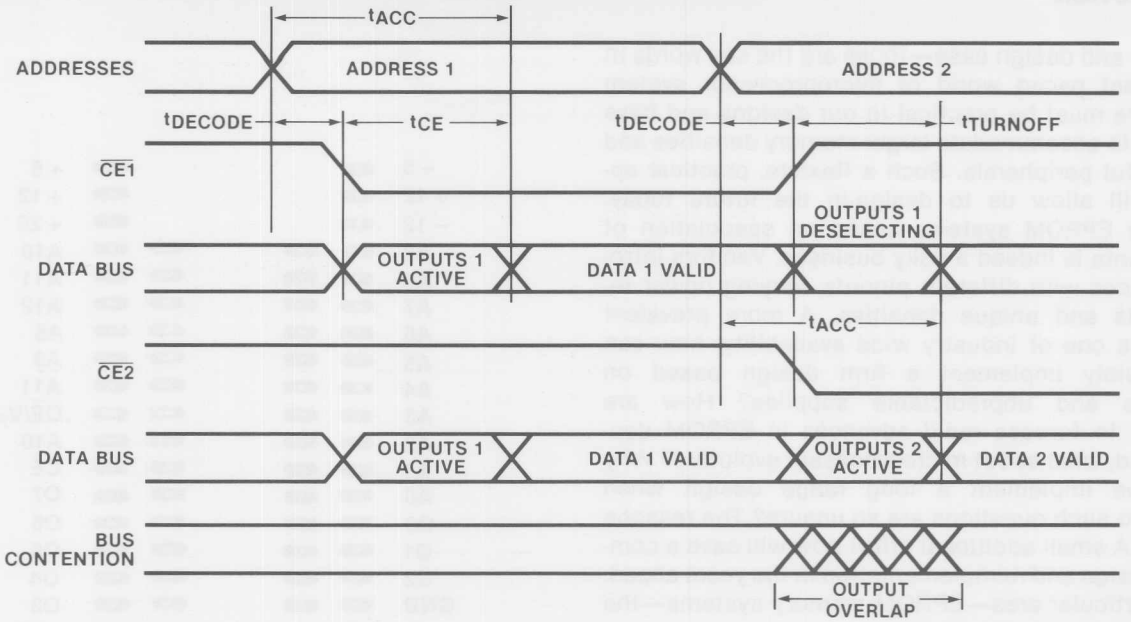


Figure 2. 1-Line Control Timing

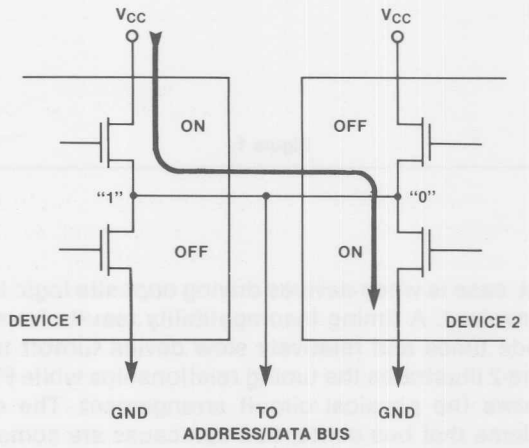


Figure 3. Bus Contention Path

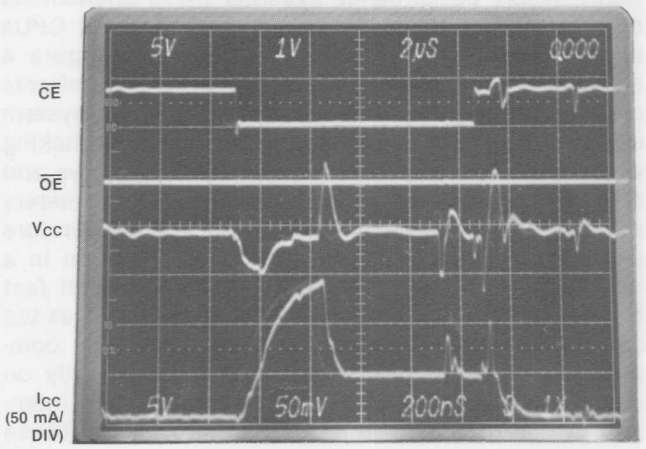


Figure 4.

Another means of device selection that completely eliminates the possibility of bus contention is a 2-line control scheme. All higher density Intel EPROMs possess this power down control architecture. Contention is eliminated through the use of an Output Enable ($\overline{OE}$) control pin. The $\overline{OE}$ line controls the EPROM's tri-state output buffer and is designed to merge directly with the microprocessor outputs. The microprocessor allows data transfer through address decode *and* system control signals (typically $\overline{RD}$ in Intel processors). Chip selection is based on address decode as before, however, the microprocessor controls when data is allowed onto the bus through the $\overline{OE}$ pin. Generous timing between addresses and output enable guarantee that no contention will exist. Figure 5 illustrates 2-line control timing; Figure 6 shows oscilloscope photographs of system operation. It is clear that 2-line control frees the designer from much of the burden in assessing system timings. In addition, the design functionability is somewhat more assured than in a single control situation. Two-line control, an attribute of Intel products, thus reduces the burden that bus contention places on the system designer.

EPROM DENSITY UPGRADES

A fundamental advantage of flexible EPROM system design is the ability to increase storage capacity without hardware modification. The optimum situation would be one in which components of higher byte densities could be plugged directly into a socket used for lower densities. This gives the designer a wide range of options to tailor his memory system size to a particular application. A universal EPROM card is then available to a broad range of different products—saving design time and hardware costs. In designing such a system, several questions need to be addressed: Are EPROMs going to

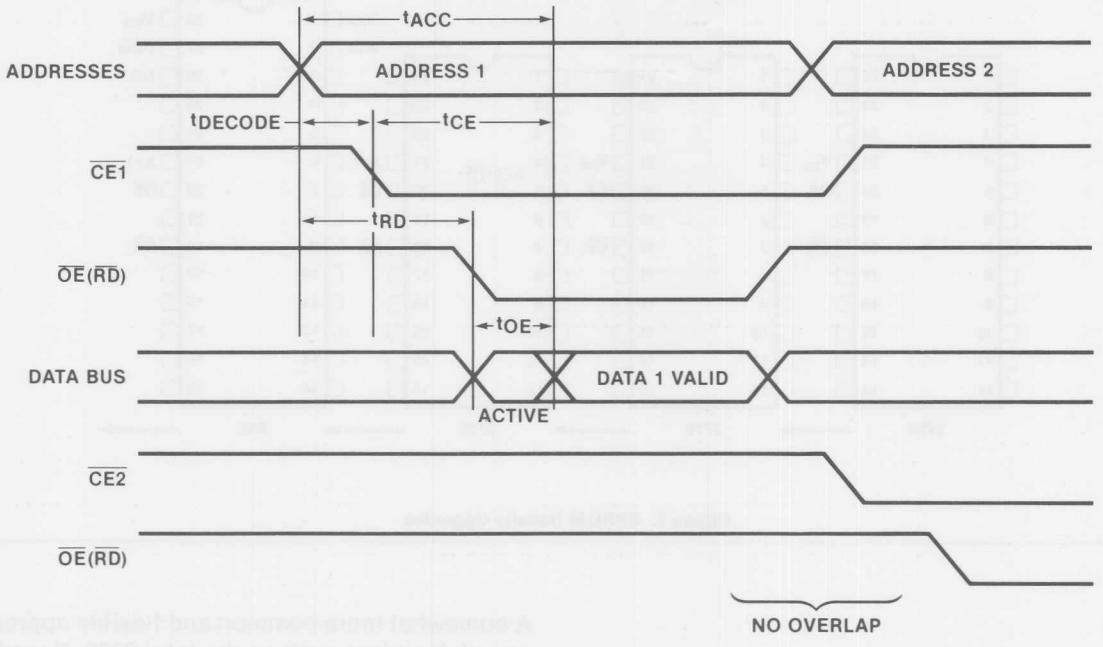


Figure 5. 2-Line Control Timing

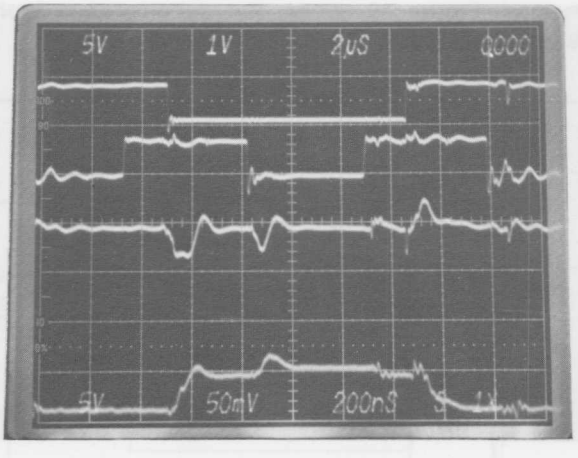


Figure 6.

be used for program store in a production mode? Are ROMs to be used to replace EPROMs during production? Is board space at a premium? Are second sources available?

Generally a present generation EPROM pinout determines the next generation ROM pinout. If one is planning to utilize ROMs in a production mode, this generality is significant. However, if EPROMs are to be used solely, one must consider the present EPROM pinout and foresee the changes that will allow higher densities. If many different pinouts become available simultaneously, we are offered a confusing choice in assessing what pinout will become a volume standard. Unfortunately, we cannot accommodate all of the possible variations.

It is generally agreed that future developments in device density will occur through the conversion to 28 pin sites; such a direction is currently favored by the JEDEC standards committee. The advantage of such an approach is that lower capacity components can be inserted directly into the 28 pin site. This leaves the user with a wide range of board level densities to choose from. Figure 7 indicates one possible upgrade path for the near term; longer range possibilities are difficult to assess. In any event, the notable feature about the 28 pin site is its ability to accommodate very large EPROM densities. The addition of 4 pins allows a factor of 16 increase over the 2732 density. This future 512K bit device will even preserve the 2-line control scheme. Admittedly, these densities are some time away, however, more powerful microprocessors are becoming available that require large storage densities.

A basic design approach involves providing addresses on the board level for the highest foreseeable density (64K bytes in this case). Switches or jumpers then allow plug compatibility for different devices. One card accommodates all densities instead of a single board matched to a particular device. The flexibility gained would allow an "off the shelf" EPROM card that could be used for simple and complex system implementations. Product life can then be protracted because board level designs are kept intact for future developments. It would seem that the incremental cost in providing 28 pin sites is small in comparison to the benefit realized.

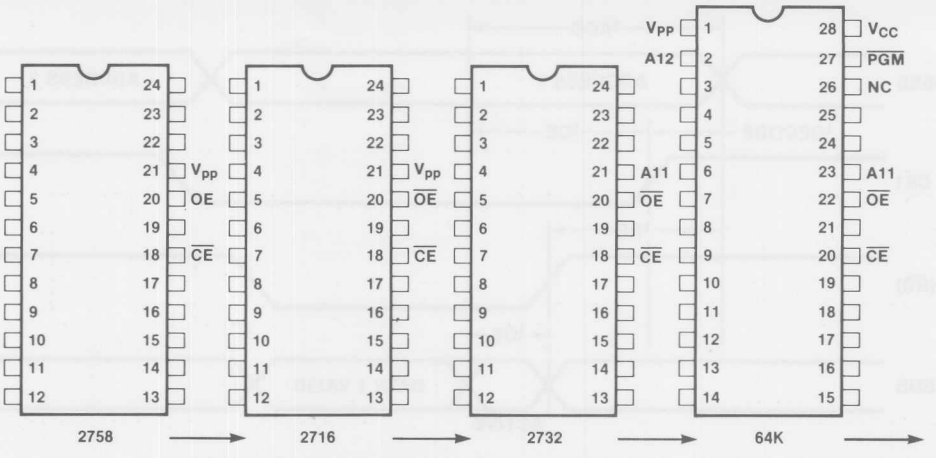


Figure 7. EPROM Density Upgrades

DECODING

Before any significant universality can be achieved, it is necessary to create a flexible decoding arrangement. Depending on the nature of the application, decoding schemes vary from the very simple to the extremely complex.

When there are few devices residing in system the most effective scheme is a simple NAND gate. Such an implementation is the lowest in cost, both from a component and power requirements standpoint. Figure 9 shows an arrangement for two devices. The major flaw with such an approach is the lack of simple density evolution. In addition, one must be careful to prevent bus contention when only using single line control (the rapid selection through the gate being the source of the problem).

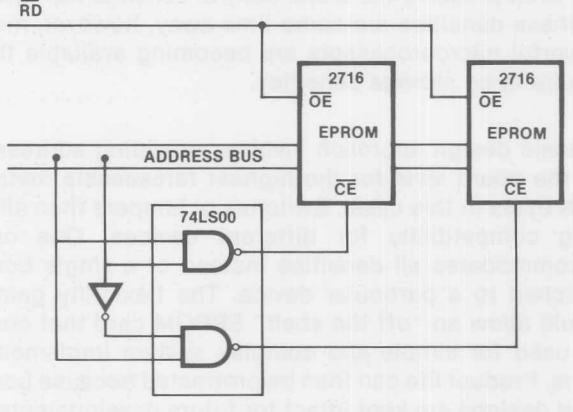


Figure 9. Nand Gate Decoding

A somewhat more common and flexible approach is the use of decoders such as the Intel 8205. Decoders allow selection of a greater number of devices yet, unfortunately, they lack the complexity to automatically compensate for changes in device density. Decoders are somewhat more expensive than single gate selection schemes. Figure 10 shows the decoder in a typical system application.

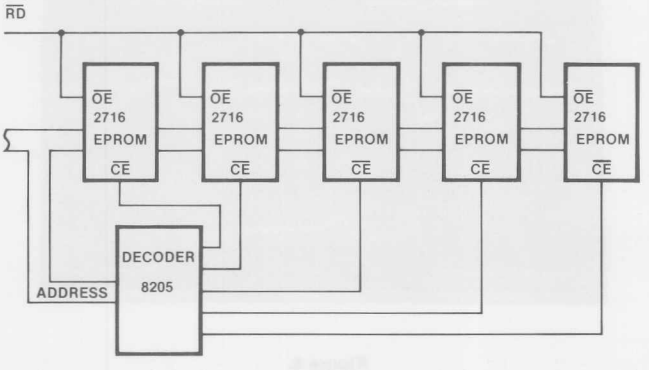


Figure 10. MSI Decoder Implementation

The most flexible means of addressing the device selection problem is an LSI approach. Dense Bipolar PROMs provide high speed as well as complex gating ability and thus offer a potent solution to direct density upgrades. The basic circuit operation allows the selection of different page boundaries, the PROM map then causes automatic segmentation. By programming the PROM with a universal decoding map, higher density parts can be inserted directly into 28 pin sites with no hardware modification. The PROM map is constructed in such a way as to maximize the number of different device densities that are plug compatible. In addition, the ability to interface 8 and 16 bit systems is also required. Figure 11

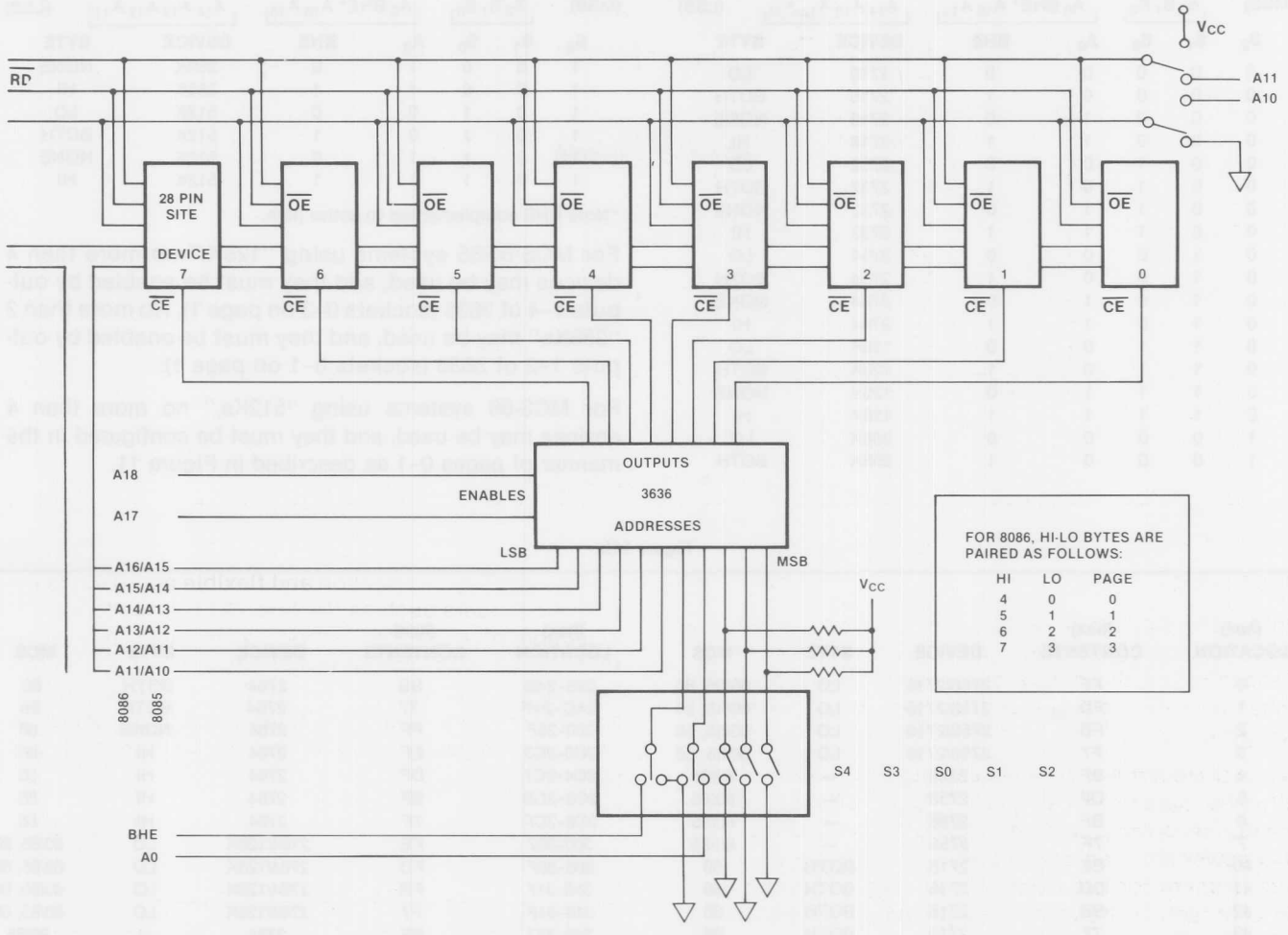


Figure 11. Universal PROM Decoder

For MCS-80/85, address input to 3636 looks like:

(MSB) $\underbrace{S_2\,S_1\,S_0}$ $\underbrace{0\,0\,A_{15}\,A_{14}}$ $\underbrace{A_{13}\,A_{12}\,A_{11}\,A_{10}}$ (LSB)

S_2	S_1	S_0	DEVICE
0	0	0	2758
0	0	1	2716
0	1	0	2732
0	1	1	2764
1	0	0	128K
1	0	1	256K

Figure 11a.

shows the hardware implementation of such a scheme; Figure 12 is a PROM map that satisfies 8085, 8086, and 8088 processor interfaces with EPROM chip densities ranging from 1K byte to 64K bytes. In 8 bit microprocessor systems the decoder will handle 2716, 2732, 64K, 128K and 256K bit devices. The maximum decode capacity is 64K bytes. For 8086 systems, devices up to 512K bits can be decoded with a maximum capacity of 256K bytes.

In practice, the user sets the decoder page boundary by selecting switches S0–S2. The mode select table relates those switch positions to the device density that is to be used in the socket. Depending on the microprocessor status (8085, 8088, or 8086), switches S3 and S4 are adjusted. These switches allow the decoder to interpret byte or word accesses in 16 bit systems. As noted before, Figure 11 details such a scheme. Figures 11a and 11b indicate the switch positions and PROM addressing for 8085 and 8086 systems.

For MCS-86, address input to 3636 looks like:

(MSB) $S_2 S_1 S_0$			A_0 BHE* $A_{16} A_{15}$		$A_{14} A_{13} A_{12} A_{11}$	(LSB)
S_2	S_1	S_0	A_0	BHE	DEVICE	BYTE
0	0	0	0	0	2716	LO
0	0	0	0	1	2716	BOTH
0	0	0	1	0	2716	NONE
0	0	0	1	1	2716	HI
0	0	1	0	0	2732	LO
0	0	1	0	1	2732	BOTH
0	0	1	1	0	2732	NONE
0	0	1	1	1	2732	HI
0	1	0	0	0	2764	LO
0	1	0	0	1	2764	BOTH
0	1	0	1	0	2764	NONE
0	1	0	1	1	2764	HI
0	1	1	0	0	128K	LO
0	1	1	0	1	128K	BOTH
0	1	1	1	0	128K	NONE
0	1	1	1	1	128K	HI
1	0	0	0	0	256K	LO
1	0	0	0	1	256K	BOTH
1	0	0	1	0	256K	NONE
1	0	0	1	1	256K	HI
1	0	1	0	0	512K	LO
1	0	1	0	1	512K	BOTH
1	0	1	1	0	512K	NONE
1	0	1	1	1	512K	HI

*Note $\overline{\text{BHE}}$ complemented to active high.

For MCS-80/85 systems using "128K," no more than 4 devices may be used, and they must be enabled by outputs 1-4 of 3636 (sockets 0-3 on page 1). No more than 2 "256Ks" may be used, and they must be enabled by outputs 1-2 of 3636 (sockets 0-1 on page 1).

For MCS-86 systems using "512Ks," no more than 4 devices may be used, and they must be configured in the manner of pages 0-1 as described in Figure 11.

Figure 11b.

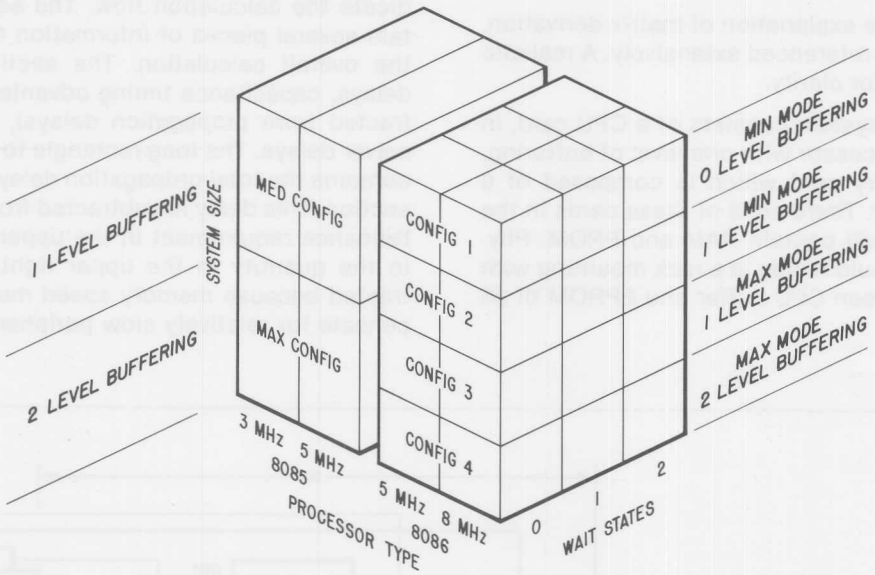
(hex) LOCATION	(hex) CONTENTS	DEVICE	BYTE	MCS	(hex) LOCATION	(hex) CONTENTS	DEVICE	BYTE	MCS
0	FE	2758/2716	LO	80/85, 86	248-24B	BB	2764	BOTH	86
1	FD	2758/2716	LO	80/85, 86	24C-24F	77	2764	BOTH	86
2	FB	2758/2716	LO	80/85, 86	280-28F	FF	2764	NONE	86
3	F7	2758/2716	LO	80/85, 86	2C0-2C3	EF	2764	HI	86
4	EF	2758	—	80/85	2C4-2C7	DF	2764	HI	86
5	DF	2758	—	80/85	2C8-2CB	BF	2764	HI	86
6	BF	2758	—	80/85	2C6-2CF	7F	2764	HI	86
7	7F	2758	—	80/85	300-307	FE	2764/128K	LO	80/85, 86
40	EE	2716	BOTH	86	308-30F	FD	2764/128K	LO	80/85, 86
41	DD	2716	BOTH	86	310-317	FB	2764/128K	LO	80/85, 86
42	BB	2716	BOTH	86	318-31F	F7	2764/128K	LO	80/85, 86
43	77	2716	BOTH	86	320-327	EF	2764	—	80/85
80-83	FF	2716	NONE	86	328-32F	DF	2764	—	80/85
C0	EF	2716	HI	86	330-337	BF	2764	—	80/85
C1	DF	2716	HI	86	338-33F	7F	2764	—	80/85
C2	BF	2716	HI	86	340-347	EE	128K	BOTH	86
C3	7F	2716	HI	86	348-34F	DD	128K	BOTH	86
100-101	FE	2716/2732	LO	80/85, 86	350-357	BB	128K	BOTH	86
102-103	FD	2716/2732	LO	80/85, 86	358-35F	77	128K	BOTH	86
104-105	FB	2716/2732	LO	80/85, 86	380-39F	FF	128K	NONE	86
106-107	F7	2716/2732	LO	80/85, 86	3C0-3C7	EF	128K	HI	86
108-109	EF	2716	—	80/85	3C8-3CF	DF	128K	HI	86
10A-10B	DF	2716	—	80/85	3D0-3D7	BF	128K	HI	86
10C-10D	BF	2716	—	80/85	3D8-3DF	7F	128K	HI	86
10E-10F	7F	2716	—	80/85	400-40F	FE	128K/256K	LO	80/85, 86
140-141	EE	2732	BOTH	86	410-41F	FD	128K/256K	LO	80/85, 86
142-143	DD	2732	BOTH	86	420-42F	FB	128K/256K	LO	80/85, 86
144-145	BB	2732	BOTH	86	430-43F	F7	128K/256K	LO	80/85, 86
146-147	77	2732	BOTH	86	440-44F	EE	256K	BOTH	86
180-187	FF	2732	NONE	86	450-45F	DD	256K	BOTH	86
1C0-1C1	EF	2732	HI	86	460-46F	BB	256K	BOTH	86
1C2-1C3	DF	2732	HI	86	470-47F	77	256K	BOTH	86
1C4-1C5	BF	2732	HI	86	480-4BF	FF	256K	NONE	86
1C6-1C7	7F	2732	HI	86	4CD-4CF	EF	256K	HI	86
200-203	FE	2732/2764	LO	80/85, 86	4D0-4DF	DF	256K	HI	86
204-207	FD	2732/2764	LO	80/85, 86	4E0-4EF	BF	256K	HI	86
208-20B	FB	2732/2764	LO	80/85, 86	4F0-4FF	7F	256K	HI	86
20C-20F	F7	2732/2764	LO	80/85, 86	500-51F	FE	256K/512K	LO	80/85, 86
210-213	EF	2732	—	80/85	520-53F	FD	256K/512K	LO	80/85, 86
214-217	DF	2732	—	80/85	540-55F	EE	512K	BOTH	86
218-21B	BF	2732	—	80/85	560-57F	DD	512K	BOTH	86
21C-21F	7F	2732	—	80/85	580-58F	FF	512K	NONE	86
240-243	EE	2764	BOTH	86	5C0-5DF	EF	512K	HI	86
244-247	DD	2764	BOTH	86	5E0-5FF	DF	512K	HI	86

Figure 12.

MEMORY PERFORMANCE CALCULATIONS AND THE MEMORY MATRIX

An extremely important factor in implementing a cost effective design is appropriate speed selection of EPROM devices. In determining required memory parameters, one must consider several factors. Processor speeds, card layout, buffer and latch delays, and capacitive loading effects all must be assessed. The following considerations are important in selecting the most appropriate and cost effective memory device.

An important decision regards the use of bus cycle wait states. If one can tolerate any number of wait state cycles, the following discussion will have little importance. However, if the decision is between none, 1, or 2 states, the memory matrix is a useful tool in making such a decision. The matrix (for Intel Microprocessors) is shown in Figure 13. It simply relates microprocessor type and system configuration to worst case memory speed requirements. The numbers in each of the matrix cells are worst case t_{CE} times. They represent the combination of all the system attributes on the matrix axis.



Access Times Requirements

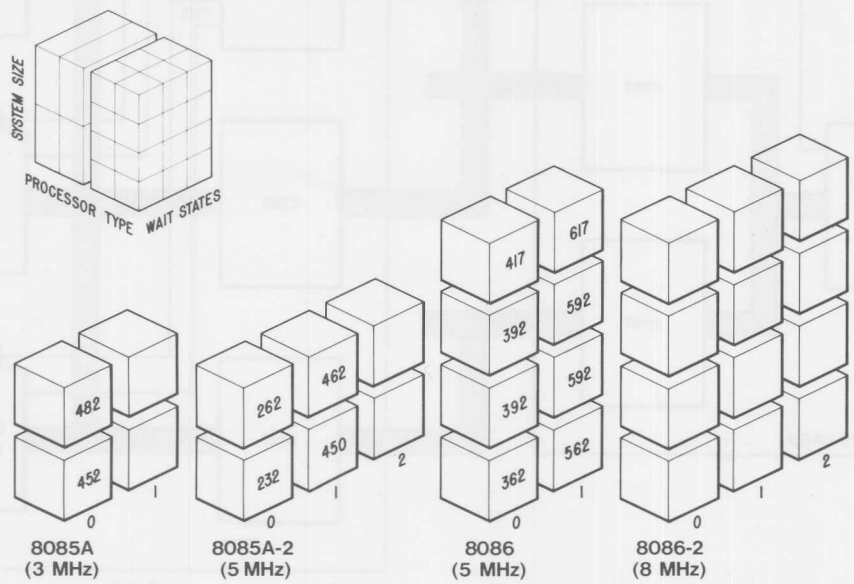


Figure 13. Microprocessor/Memory Matrix

To generate such a number array one must have a fairly complete understanding of the memory microprocessor interface. We will consider the system in Figure 14 and the relevant data paths noted there. The access scenario is as follows: The microprocessor issues an address onto its address/data bus. The multiplexed address is latched, and delayed; the address may be delayed further by bus drivers. The address is then decoded (another delay) and $\overline{CE}$ reaches the memory device. Valid data then appears on the device output pins after t_{CE}. This data is propagated and delayed through levels of data transceivers and finally reaches the microprocessor. Depending on the circuit arrangement, wire lengths may increase these delays, and small capacitive loading may decrease them. The buffer and latch blocks may be several layers deep to accommodate different system sizes and applications.

To provide a complete explanation of matrix derivation, Figures 15 and 16 are referenced extensively. A realistic example is provided for clarity.

The microprocessor system consists of a CPU card, in this case an 8086 processor with one level of buffering, and a remote memory card which is composed of 6 EPROMs and a buffer. There are 8 of these cards in the system, some of which contain RAM and PROM. Physically, the system could reside in a rack mounting with a total distance between CPU buffer and EPROM of 36 inches.

Two calculations will be discussed—memory performance requirements and system timing margins. The memory performance parameters under consideration are t_{ACC} and t_{CE}. The output enable time t_{OE} can be calculated in a similar manner. We will proceed as follows:

1. Determine the processor requirements.
   - Time from addresses to data valid
2. Determine time from addresses to CE.
   - Consider propagation delays
   - Consider capacitive effects
   - Consider wiring delays
3. Determine the propagation delay from memory device to microprocessor.

Referring now to Figure 15. Arrows within data paths indicate the calculation flow. The sectioned boxes contain several pieces of information that are pertinent to the overall calculation. The sections contain wiring delays, capacitance timing advantages (which are subtracted from propagation delays), and latch or transceiver delays. The long rectangle to the immediate right contains the total propagation delay through that circuit section. This delay is subtracted from the incoming performance requirement in the upper left box—resulting in the quantity in the upper right. The delay is subtracted because memory speed must increase to compensate for relatively slow peripherals. The calculation

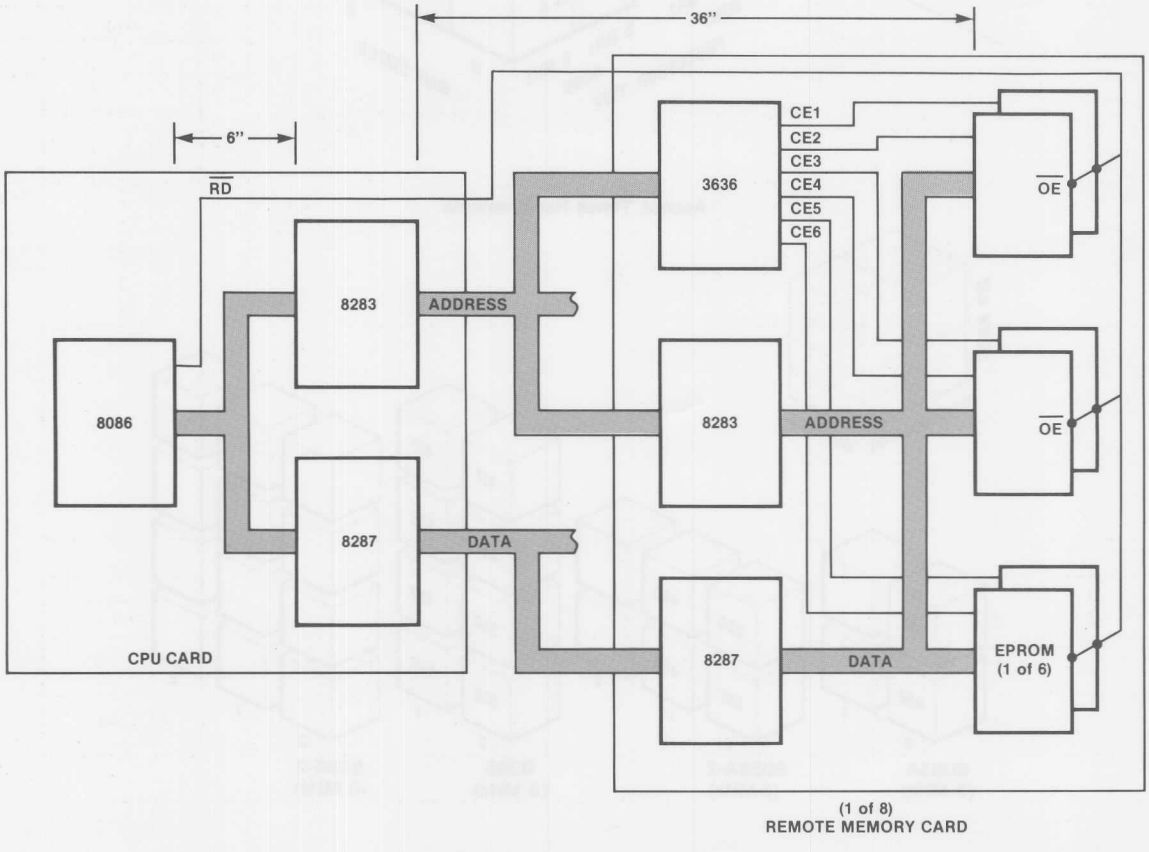


Figure 14. Timing Example

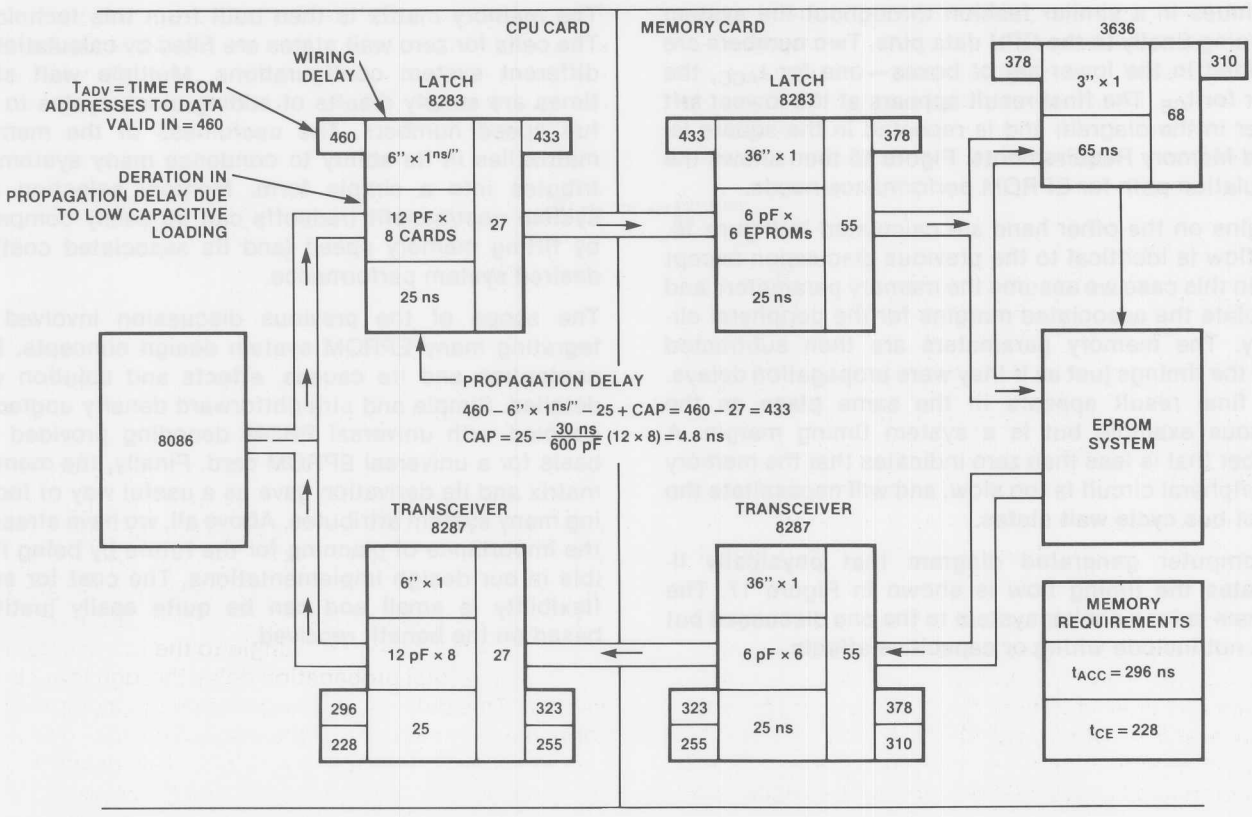


Figure 15. Memory Requirements Timing Flow

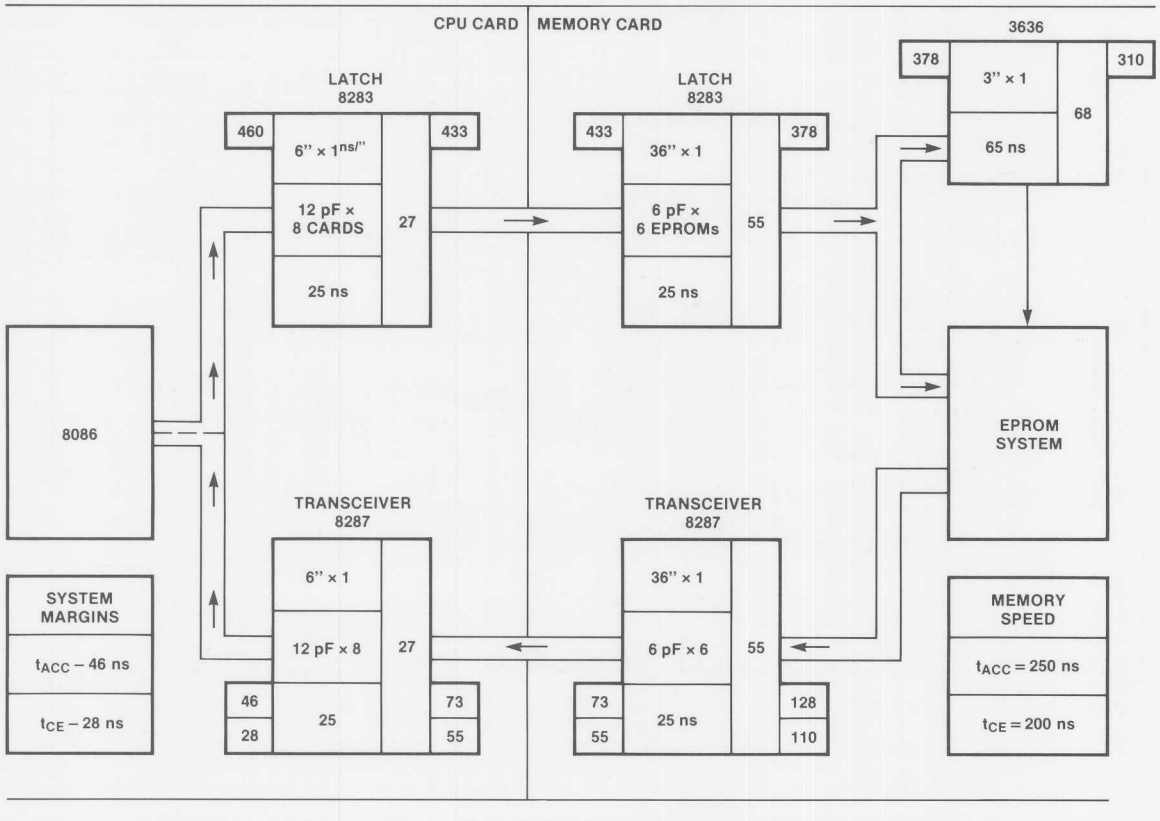


Figure 16. System Margins Timing Flow

continues in a similar fashion throughout the system returning finally to the CPU data pins. Two numbers are provided in the lower set of boxes—one for t_{ACC}, the other for t_{CE}. The final result appears at the lowest left buffer in the diagram and is repeated in the square labeled Memory Requirements. Figure 15 then shows the calculation path for EPROM performance needs.

Margins on the other hand are calculated in Figure 16. The flow is identical to the previous discussion except that in this case we assume the memory parameters and calculate the associated margins for the peripheral circuitry. The memory parameters are then subtracted from the timings just as if they were propagation delays. The final result appears in the same place as the previous example but is a system timing margin. A number that is less than zero indicates that the memory or peripheral circuit is too slow, and will necessitate the use of bus cycle wait states.

A computer generated diagram that physically illustrates the timing flow is shown in Figure 17. The diagram is for a similar system to the one discussed but does not include wiring or capacitive affects.

The memory matrix is then built from this technique. The cells for zero wait states are filled by calculation of different system configurations. Multiple wait state times are simply results of adding clock cycles to the full speed numbers. The usefulness of the memory matrix lies in its ability to condense many system attributes into a simple form. Memory selection and system cost/benefit tradeoffs can be easily compared by fitting memory speed (and its associated cost) to desired system performance.

The scope of the previous discussion involved integrating many EPROM system design concepts. Bus contention and its causes, effects and solution was detailed. Simple and straightforward density upgrades, coupled with universal PROM decoding provided the basis for a universal EPROM card. Finally, the memory matrix and its derivation gave us a useful way of focusing many system attributes. Above all, we have stressed the importance of planning for the future by being flexible in our design implementations. The cost for such flexibility is small and can be quite easily justified based on the benefit received.

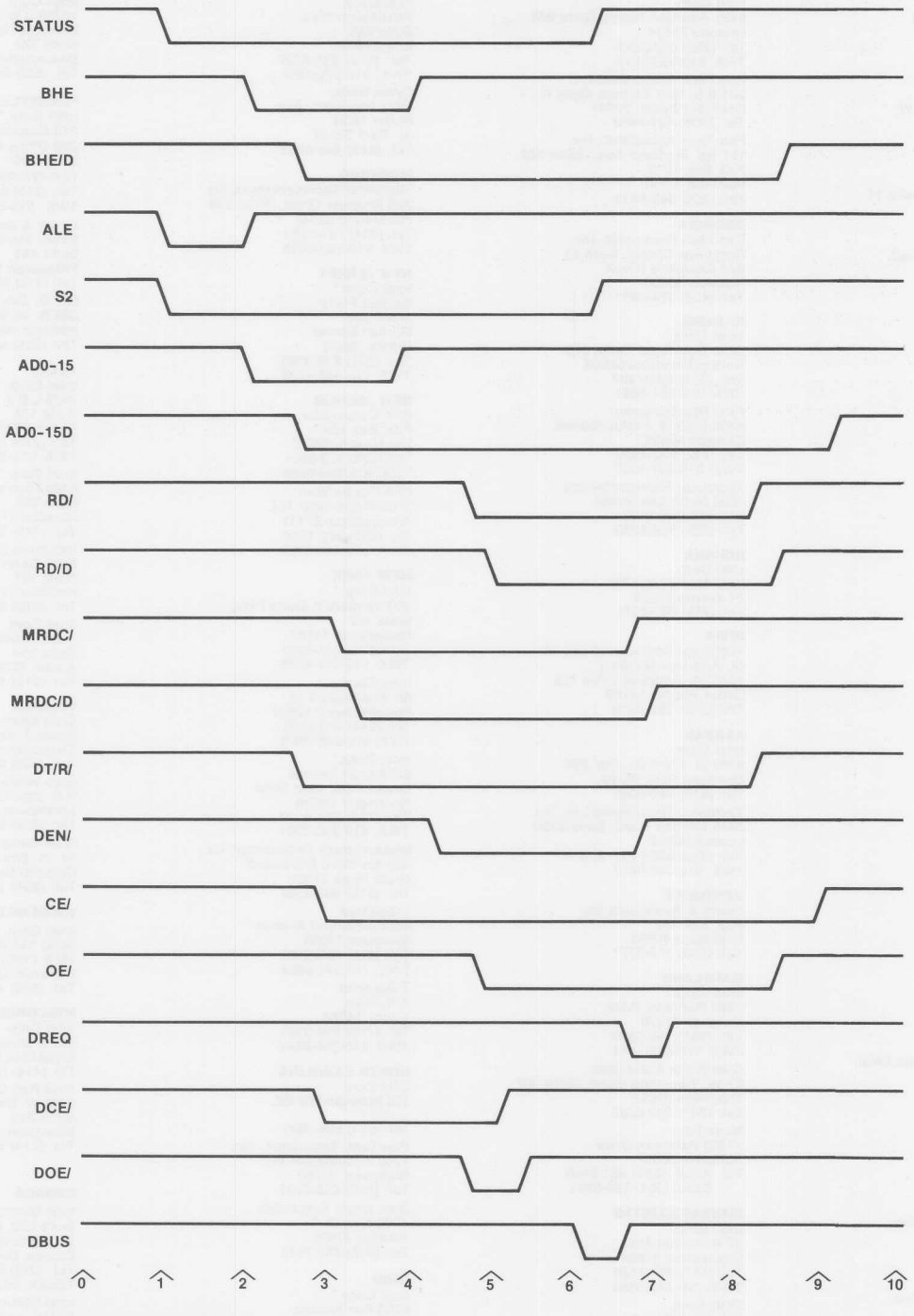


Figure 17. 8086 Configuration 4, 3625 Decode

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